Design and Simulation of Duobinary Encoder Circuit for Communication System

R. R. Mahmud, M. A. G. Khan, S. M. A. Razzak

Abstract—This paper presents microcontroller based schematic circuit design with simulation results of a duobinary encoder (duobinary code from binary bit) for data communication system. Binary code has two levels of bit sequence that are 1 and 0. On the other side, duobinary (DB) is a three-level code that is 1, 0 and -1 level. Microcontroller based duobinary encoder can encode the binary signal to duobinary signal by simple circuit operation. The three bits comparison part of the encoding technique can be done by microcontroller portion very easily. Using duobinary transmission instead of binary transmission, it can improve the system performance and bandwidth efficiency of output signal.

Keywords— Duobinary Encoder, Duobinary Decoder, Microcontroller, Two Input Inverting Adder.

1 Introduction

An efficient use of channel bandwidth is achieved through duobinary coding scheme. A binary data stream can be encoded into a duobinary signal (three level data (1, 0, -1)) simply by adding the binary data stream with its one bit delayed stream or by precoding technique. Duobinary transmission was first invented in 1960 but applied on 1990 in the fiber optic communication [5]. The advantages of duobinary transmission over binary transmission are: (a) it has a narrower bandwidth than binary format; (b) it has a greater spectral bandwidth; (c) It suffers less than Stimulated Brillouin Scattering (SBS); (d) Easy to implement and (e) the average power level of duobinary signal is less than the average power level of binary signal. Our topic is different from the other researchers who have done their research on the same area. To show in difference between our findings and others, we would like to explain their researches. One of the researchers Jiang who have shown that the complexity setup to the transmitter portion can be reduced by using a single-arm Mach-Zender modulator (MZM) for bandwidth 10 GB/s and for 252 km of uncompensated standard single mode fiber (SSMF) [6]. A 3 dB bandwidth of Bessel Low Pass Filter could be used to generate electrical duobinary signals for 40 GB/s duobinary system which was designed by A. Rahman et al [9]. In 2008, Y. C. Lu et al demonstrated that 100% driving voltage did not need for optimal duobinary system [4]. All the mentioned papers explained about the performance of duobinary transmission, the bandwidth of low pass filters and modulation technique of communication system. But so far as we know that there is no paper explains about this duobinary encoder technique with detail circuit design and simulation results. So our paper is unique that is microcontroller based schematic circuit design and simulation of a complete duobinary encoder (duobinary code from binary bit) for data communication system. One example of duobinary encoder and decoder bit sequence from binary is given below in Figure 1.

Binary	1	1	0	1	1	0	0	1
NOT	0	0	1	0	0	1	1	0
EXOR	0	0	1	1	1	0	1	1
X	0	0	1	1	1	1	1	1
Y	1	1	1	0	0	1	1	0
Duobinary								
E_k	0	0	0	1	1	0	0	1
F_k	0	0	1	1	1	1	1	1
$\bar{A}$	0	0	1	0	0	1	1	0
A/Binary Orginal	1	1	0	1	1	0	0	1

Figure 1: Example of a duobinary encoder and decoder bit sequence from binary bit stream.

2 Duobinary Encoder

The duobinary encoding technique is a part of transmitter portion. First binary bit is generated. Then it is encoded to duobinary bit sequence which is given below in Figure 2.

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2.1 Block Diagram of a Duobinary Encoder

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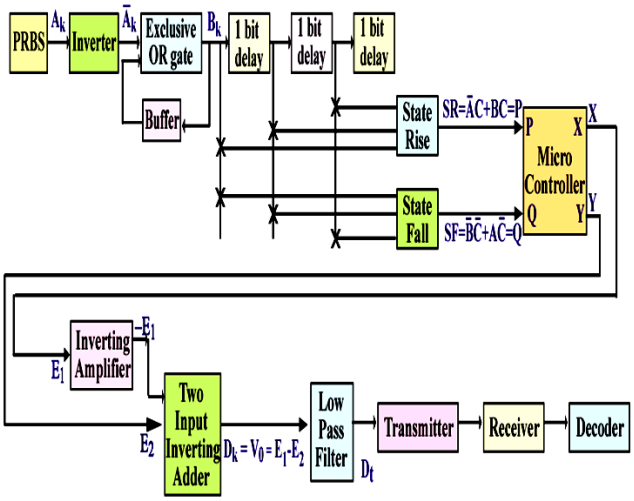


Figure 2: Block diagram of conversion technique from binary to duobinary code and total communication system (encoder and decoder).

2.2 Algorithm of Duobinary Encoder

The conversion technique from binary to duobinary bit stream follows some rules called algorithm which is given below.

Step 1: It contains three level means 1, 0, -1.
Step 2: Duobinary code depends on comparison of every 3 bit numbers for each and every position.
Step 3: If the neighbor 2 bits among 3 bits are same then it tends to change the state. If it is not same then it holds the level means 0 level.
Step 4: Initially the level starts from -1.
Step 5: If the signal is on state 1 and getting signal of state rise then it will be on state 1 level because 1 is the highest level in positive side.
Step6: Similarly, if the signal is on state -1 and getting signal of state fall then it will be on state -1 level because -1 is the lowest level in negative side.

2.3 Description of Duobinary Encoder

Pseudo Random Bit Sequence (PRBS) is a binary bit generator that generates binary data of two levels (1 and 0). The data will be random and the time delay of the bit gap is fixed for an interval. The PRBS is inverted by applying NOT logic gate. The precoding output has two levels of bit sequence that is 1 and 0 which can be achieved by applying an exclusive-or (XOR) gate. Among the two inputs of the XOR gate, one is the output of NOT gate and another is the previous bit of exclusive-or gate. So 1 bit delay can be done by using a single D flip-flop. From the truth table 1, it is observed that state changing is followed from the second bit to the third bit of the precoded bit showing by arrow. When 1 comes after 0 and among 3 bits two 1's or two 0's are neighbor then it will be state rise. But when 0 comes after 1 and among 3 bits two 1's or 0's are neighbor then it will be state fall. Besides these for 101 and 010, it will be state hold because among 3 bits two 1's or 0's are not neighbor. When state rise and state fall are not active then it will be state hold means 0 level. From the table Karnaugh map can be obtained by the case of sum of product (SOP).

TABLE 1
TRUTH TABLE OF THE COMPARISON OF DUOBINARY CODING STATE WITH EVERY THREE BITS

A	B	C	STATE CONDITION
0	0	0	State fall
0	0	1	State rise
0	1	0	State hold
0	1	1	State rise
1	0	0	State fall
1	0	1	State hold
1	1	0	State fall
1	1	1	State rise

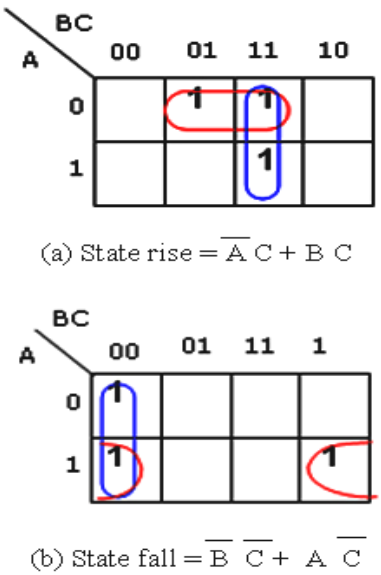


Figure 3: Karnaugh map and logical equation for (a)state rise and (b)state fall of duobinary encoding technique.

3 Microcontroller Based Duobinary Encoder Circuit

Microcontroller is a programmable device which contains a microprocessor, random access memory (RAM), read only memory (ROM), registers etc as same as single chip computer. As microcontroller is a low cost programmable device, it is used in the automatic control application. For example robot, microwave oven, digital watch, mobile phone, electronic display and some conditions where logical circuit operation is difficult. Algorithm of the assembly language program for microcontroller of duobinary encoder is given below. Atmega32 type microcontroller is used in simulation circuit.

3.1 Algorithm and flow chart of the Assembly Language Program

Step 1: Initialize the segment arrangement.
Step 2: Initially output port will be -5 volt.
Step 3: Take previous state data from output port for determine state condition.
Step 4: Take next state data from input port.
Step 5: Compare the input port data with previous state for step up, step down and step hold.
Step 6: Give the output data to the output port.
Step 7: Loop
Step 8: End

For converting from precode to duobinary encode a micro controller atmega32 is used. Two input ports (P, Q) and two output ports (X, Y) are need for this program. Let PPIA and PPIB are the output ports represent X and Y. On the other side PPIC and PPID are the input ports represent P and Q in the program. The truth table of the program that follows the rule to convert precode to duobinary code is given in the table 2. Initially the output port should be started from -1 level means state fall representing PPIA=0 and PPIB=1. For PPIA =0/1 and PPIB = 0/1 represent 0 level means state hold and PPIA=1 and PPIB=0 represent 1 level means state rise. After initialization the encoded bit from -1 level, the program will take the previous output bits from PPIA to the base register lower side BL and PPIB to the base register upper side BH. Then compare PPIA with PPIB by subtracting. If PPIA is less than PPIB then it means the code is on -1 level and it goes to the L_1 level of the program. If PPIA is greater than PPIB then it means the code is on 1 level and it goes to the L_4 level of the program and for PPIA is equal to PPIB, the program goes to the level L_7.

TABLE 2
TRUTH TABLE OF MICROCONTROLLER INPUT AND OUTPUT STATE CONDITION OF ASSEMBLY LANGUAGE PROGRAM FOR DUOBINARY ENCODING TECHNIQUE

INPUT PORT: P, Q				OUTPUT PORT: X, Y	
PREVIOUS STATE		*INPUT DATA*		*NEXT STATE*	
X-1	Y-1	P	Q	X	Y
0	1	0	1	0	1
0	1	0	0	0/1	0/1
0	1	1	0	0/1	0/1
0/1	0/1	0	1	0	1
0/1	0/1	0	0	0/1	0/1
0/1	0/1	1	0	1	0
1	0	0	1	0/1	0/1
1	0	0	0	0/1	0/1
1	0	1	0	1	0

After that take the input codes PPIC to the data register lower side DL and PPID to the data register upper side DH respectively and then making comparison AL=DL-DH. If PPIC is less than PPID then the output port will tend to fall the state. If PPIC is equal to PPID give the result will tend to hold 0 level. If PPIC is greater than PPID the output port will tend to rise level according. If the previous bit PPIA is equal to PPIB then the state is on 0 level and it will change its level according to the input bits of PPIC and PPID. If the port value PPIC is equal to PPID then the output port PPIA will be 1/0 and PPIB will be 1/0 means state hold. If the previous bit PPIA is greater than PPIB then the state is on 1 level and it will change its level according to the input bits of PPIC and PPID. If PPIC is greater than PPID then the coding bit will be on 1 level. If the PPIC is less than PPID value then it will be 0 level. If the port value PPIC is equal to PPID then the output port PPIA will be 1/0 and PPIB will be 1/0 means state hold. If the previous bit PPIA is less than PPIB then the state is on -1 level and it will change its level according to the input bits of PPIC and PPID. If PPIC is greater than PPID then the coding bit will be on 0 level. If the PPIC is less than PPID value then it will be the level -1. If the port value PPIC is equal to PPID then the output port PPIA will be 1/0 and PPIB will be 1/0 means state hold.

In this way the program compares 3 bits numbers each and every time and gives the output result until the interrupt code is active. After this programming three types of output bits to the output ports PPIA = X and PPIB = Y can be obtained.

TABLE 3
THREE CASES OR LEVELS OF DUOBINARY ENCODER

First case	X = 1, Y = 0	State rise = 1 level
Second case	X = 1/0, Y = 1/0	State hold = 0 level
Third case	X = 0, Y = 1	State fall = -1 level

From the above table 3 these outputs of PPIA and PPIB have the values of positive and zero level logic voltage. But we need negative level logic means -1 level but there is no logic gate which will give -1 logic output. So we have to apply these programming outputs to the circuits called inverting amplifier and two inputs inverting adder circuit which is given below and finally 1level, 0 level and -1level logic voltage of duobinary coding can be obtained from the output of two inputs inverting adder circuit which is given below in the Table 4.

TABLE 4
TRUTH TABLE THAT FOLLOWS THE DUOBINARY THREE (1, 0,-1) LEVEL OF THE TWO INPUT INVERTING ADDER

Input				Output
X	Y	E_1	E_2	
0	1	0	1	- 1 level
0/1	0/1	0/1	0/1	0 level
1	0	1	0	1 level

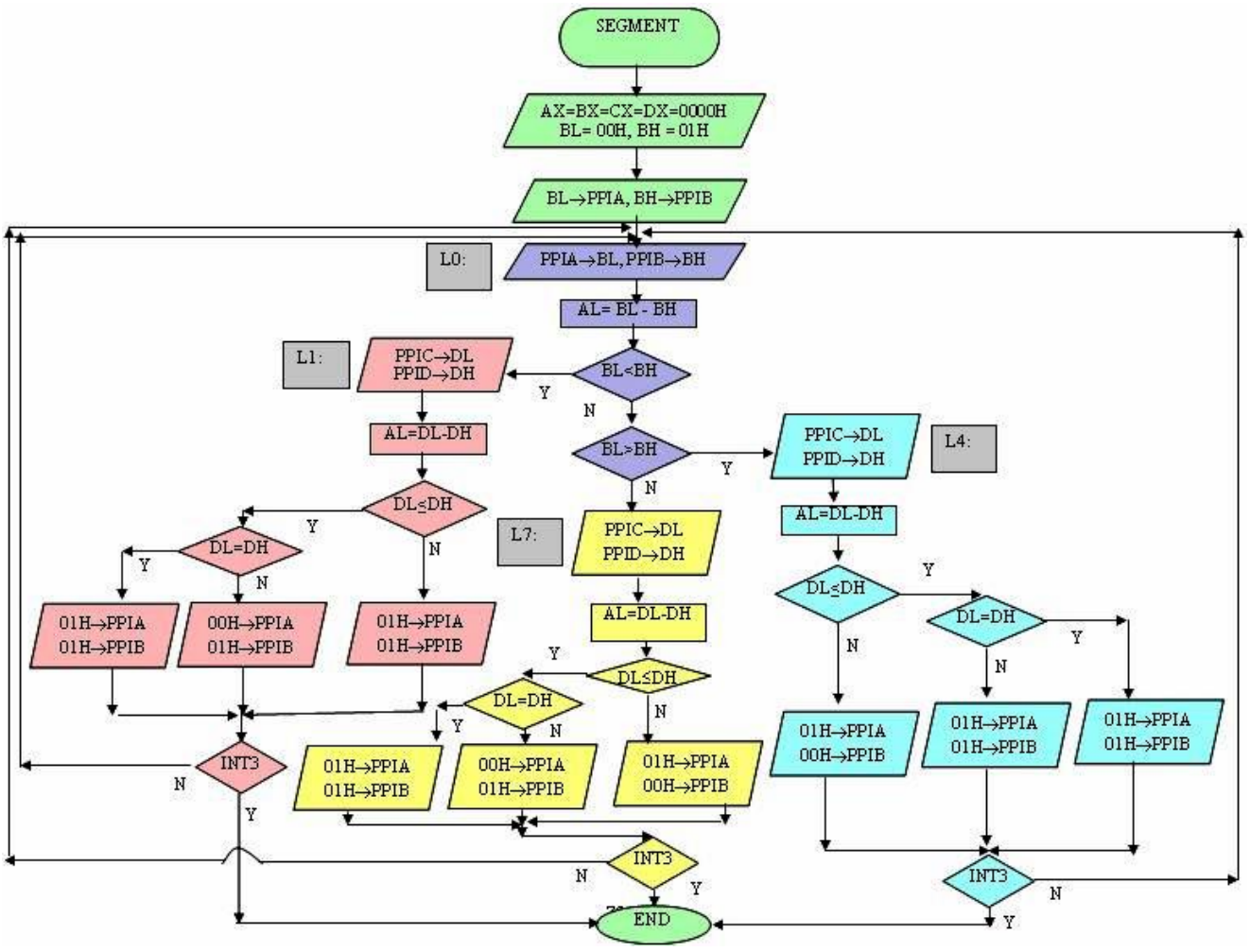


Figure 4: Flow chart of assembly language program

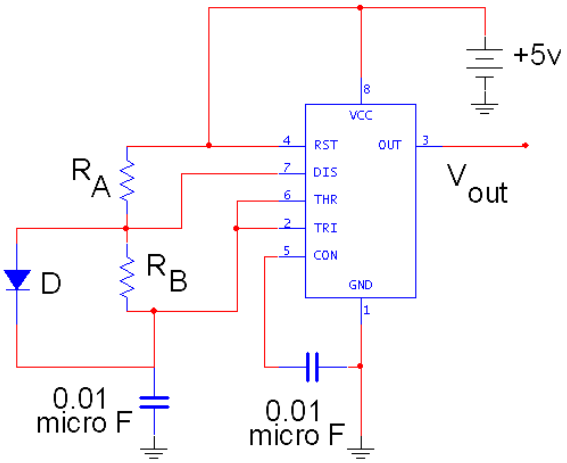
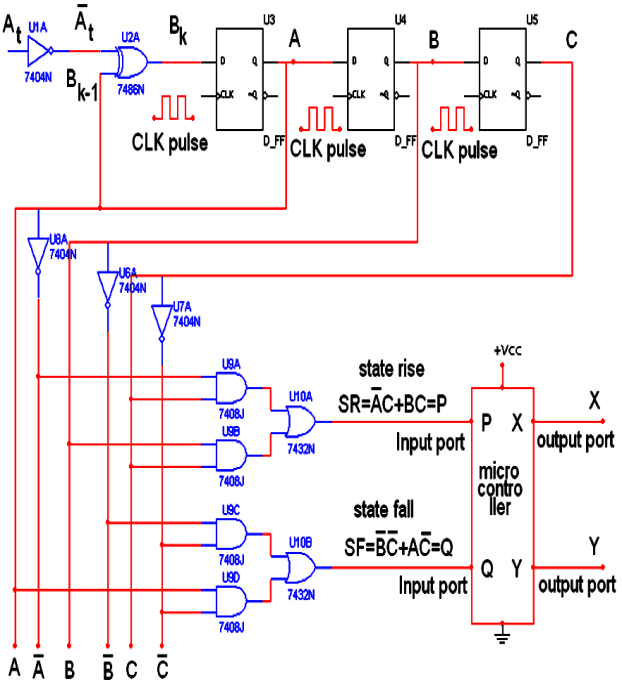


Figure 5: Schematic diagram of a clock pulse generator circuit (astable multivibrator)

From Figure 5 the duty cycle of the clock pulse can be changed by varying R and C. The frequency of the pulse is

$$f = \frac{1}{0.695(R_A + R_B)C} \quad (1)$$



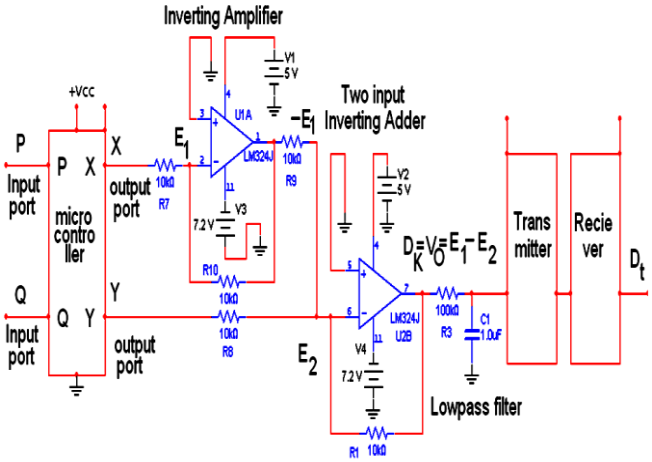


Figure 6: Schematic full circuit diagram of duobinary encoding system from binary

4 Wave Shapes and Results

Figure 7 is the simulation result by Protious 7.6 simulation software. The yellow shape of duobinary encoder represents X, blue shapes represents Y and red shape represents duobinary code in Figure 6 which is the example of Figure 1.

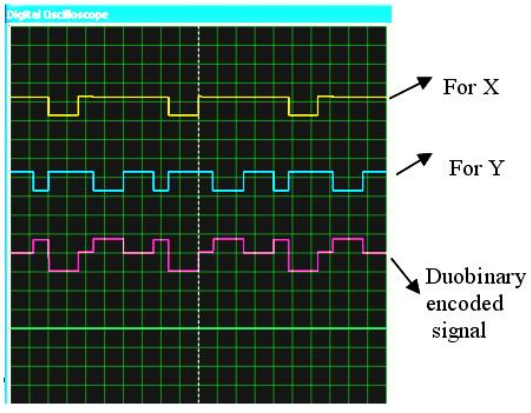


Figure 7: Simulation result of duobinary encoder

5 Conclusion

The design circuit for duobinary encoder can be implemented any required place in communication system as duobinary has greater advantages than binary format. Our microcontroller based duobinary encoder generates low average power and that is why it can travel long distance in communication system. The circuit generates duobinary data at Mbps speed. For using microcontroller, the circuit becomes simple for the three bits comparison portion and additional clock pulse is not need to the above circuit. Our circuit gives hundred percent accurate results which are given in Figure 7 with respect to the time interval and bit sequence.

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