GLFSR-Based Test Processor Employing Mixed-Mode Approach in IC Testing

Mohammod Akbar Kabir, Md. Nasim Adnan, Lutful Karim

Abstract—Integrated circuits (ICs) are the key components of all electronic equipment. Design density and complexity of the problem relating to testing ICs have become a challenge with reliable performance and low cost. Stored pattern Built-in self-test (BIST) environment suffers from high hardware overhead due to the requirement of memory devices to store previously generated test patterns. In pseudorandom BIST, environment test patterns are generated by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) which requires very little hardware overhead. LFSR requires long test sequence resulting long time in IC testing for achieving high fault coverage. In this paper, we proposed a design and investigate the performance of Generalized Linear Feedback Shift Register (GLFSR) based test processor implementing mixed-mode testing technique. It shows that GLFSR based Test processor with mixed-mode technique will enhance the performance of IC testing.

Keywords — Automatic Test Equipment (ATE), Built-in Self-Test (BIST), Circuit-Under-Test (CUT), Generalized Linear Feedback Shift Register (GLFSR), Pseudo-Random Vector (PRV).

1 INTRODUCTION

WITHthe dramatic improvement and refinement of integration technology, the design densities and associated complexities of Integrated Circuit (IC) are rapidly increasing. Continued scaling feature sizes have made the integration of several cores in a single monolithic integrated circuit possible, called system on a chip (SOC). As the number of cores integrated in a SOC increased rapidly, both the test data storage requirements on the tester and the test bandwidth requirements between the tester and the chip have grown dramatically [1]. It is expected that this growth will continue in full force in the coming years [2]. In IC manufacturing various physical defects may occur during numerous production stages. Due to the complexities in today's IC, the problems of IC testing have become much more complex. Conventional computer controlled Automatic Test Equipment (ATE) based IC testing suffers from the number of serious drawbacks such as high equipment cost, slow test speed, huge memory space to store and to process test data, and yield loss due to inaccuracy [3-4]. Built-in self-test (BIST) is an efficient testing procedure in which test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware. Stored pattern BIST suffers from high hardware cost due to memory requirement to store pre-computed test patterns. Pseudo-random BIST, where test patterns are generated by pseudo-random pattern generators such as linear feedback shift registers (LFSRs) and cellular automata (CA), requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR or CA often requires unacceptably long test sequences thereby resulting in prohibitively long test time. Linear Feedback Shift Register (LFSR) based test processor ASIC design for low cost IC testing employing weighted random approach have been reported [5-10]. In this approach, generated patterns are biased to improve the fault coverage. Test processor ASIC design employing mixed-mode technique has been proposed where Easy-to-detect (ETD) faults are detected using LFSR generated test patterns and the rest of the Hard-to-detect (HTD) faults are detected using deterministic test patterns and thereby achieved high fault coverage [11-16]. Mixed-mode testing approach is compatible with scan design and offers reduced storage requirements, shorter test application time and simple structure of hardware. It is shown that GLFSR produces quality pseudo-random vector (PRV) which in turn result acceptable fault coverage using lower number of test vectors [17]. GLFSR is outperforms the LFSR. In this paper we have proposed GLFSR based test processor employing mixed-mode technique in IC testing. The next part of this paper is organized as follows. Section 2 starts with the concept of LFSR, GLFSR and mixed mode testing, section 3 presents proposed IC testing approach, sections 4 explores test result and finally the paper ends with conclusion in section.

- *Mohammod Akbar Kabir works with the Department of Economics, University of Dhaka, Bangladesh. E-mail: akbar_kabir03@yahoo.com.*
- *Md. Nasim Adnan works with the Department of Computer Science and Engineering, University of Liberal Arts Bangladesh (ULAB), Dhaka. E-mail: nasim_1547@yahoo.co.uk.*
- *Lutful Karim is a Ph.D. student at the University of Guelph, Canada. E-mail: sumon_lk@yahoo.com.*

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2 OVERVIEW

2.1 Linear Feedback Shift Register (LFSR)

Linear feedback shift register (LFSR) is usually used to generate pseudo-random test vectors. An LFSR is a series configuration of D flip-flops and exclusive-OR (XOR)

gates. The XOR gates and shift register act to produce a Pseudo Random Binary Sequence (PRBS) at each of the flip-flop outputs.

Its operation is based on principle of polynomial arithmetic in cyclic coding theory. The general structure of n-bit LFSR is shown in Figure 1. $a_{n-1}, a_{n-2}, \ldots\ldots a_0$ are the outputs of n flip-flop of the n bit shift register and a_n is input to the shift register, equal to the exclusive-OR of the feedback signals; that is:

$$a_n = \sum a_i c_i = a_n c_n \oplus a_1 c_1 \oplus \ldots \oplus a_{n-1} c_{n-1}$$

Here the coefficient $c_i=1$ if the flip-flop output a_i is fed back to LFSR input and $c_i=0$ if a_i is not connected to the feedback circuit.An n-bit LFSR has at most 2^n states but all zero-state is prevented because the LFSR would never leave this state. Hence an n-bit LFSR can have 2^n-1 values. By correctly choosing the points at which we take the feedback from an n -bit shift register we can produce a repeatable PRV sequence of length 2n – 1, a maximal-length sequence that includes all possible patterns (or vectors) of n bits, excluding the all-zeros pattern.

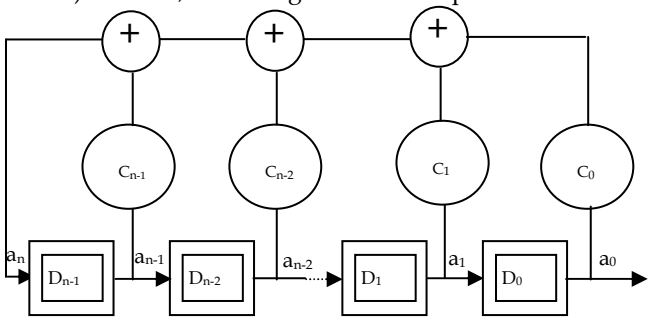
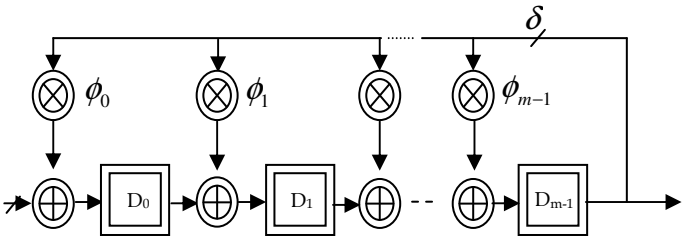


Figure 1: The general structure of LFSR.

2.2 Generalized Linear Feedback Shift Register (GLFSR)

GLFSR are generalized LFSRs that are defined over Galois field $GF(2^\delta)$, $\delta \geq 1$. It has been shown that GLFSR is significantly more effective as a test pattern generator, providing better fault coverage than the standard LFSR. The general structure of the GLFSR (δ, m) is illustrated in Figure 2. The circuit under test (CUT) is assumed to have $n = (\delta \times m)$ inputs driven by the outputs of the GLFSR. A GLFSR (δ, m) have m stages $D_0, D_1, \cdots, D_{m-1}$, where each stage has δ storage cells of shift registers. Each shift shifts δ bits from one stage to the next stages.



$GF(2^\delta)$ Adder $GF(2^\delta)$ Multiplier $GF(2^\delta)$ Storage Element

Figure 2: The general structure of GLFSR.

The feedback polynomial of a GLFSR with m stage can be represented as

$$\phi(x) = \phi_0 + \phi_1 x + \phi_2 x^2 + \ldots + \phi_{n-1} x^{m-1} + x^m$$

The coefficients of the polynomial $\phi(x)$ are elements over $GF(2^\delta)$ and define the feedback connections. The i^{th} coefficient, ϕ_i multiplies the feedback input over $GF(2^\delta)$, which can be realized using only XOR gates. The GLFSR has different structure depending on the "m" and "δ" value. To generate patterns for a circuit of n inputs, a variety of GLFSR (δ, m) is available, where $(m \times \delta) \geq n$. Different values of δ and m create different types of GLFSRs, capable of generating different types of patterns for the same n-input circuit. As the value of δ increases, the number of XOR gates needed to realize the generator increases. It has been shown that GLFSR is significantly more effective as a test pattern generator [16], providing better fault coverage than the standard LFSR. In the proposed IC testing approach Generalized Linear Feedback Shift Register (GLFSR) in place of LFSR has been used as pattern generator.

2.3 Mixed-mode Testing

Mixed-mode pattern generation includes generation of pseudo-random vectors first and then generation of deterministic test vectors. This approach exploits advantages of both the pseudo-random test technique and deterministic test technique. A generalized scheme of mixed-mode technique is shown in Figure 3. PRV generated form LFSR or other generators can cover a large percentage of easily testable faults. The remaining random pattern resistant faults are Hard-To-Detect (HTD), deterministic test vectors are then generated using same generator and tested. Thereby complete faults coverage can be achieved by this mixed-mode approach. This approach also offers reduced storage requirements, shorter test application time, and smaller area overhead compared to weighted random approach.

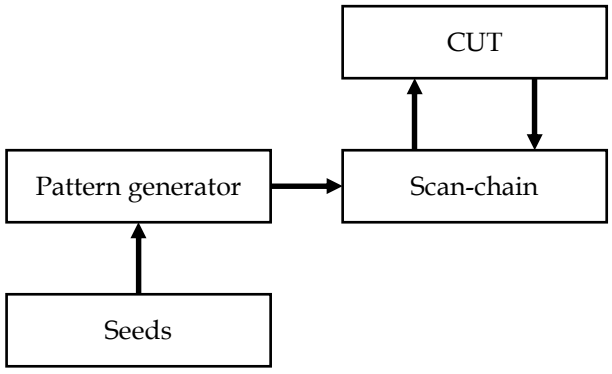


Figure 3: Generalized scheme of mixed-mode technique.

3 Proposed IC Testing Approach

In this section a complete design of GLFSR based IC test processor implementing mixed-mode testing approach has been presented. This proposed design describe a highly randomized, low hardware overhead test pattern generator (TPG) for scan-based built-in self-test (BIST) and also achieve very high fault coverage. GLFSR generated PRV is applied to a CUT to detect all the ETD faults

and then deterministic test sets are generated using the same GLFSR to target the remaining HTD faults using compacted test data called seed. Therefore complete fault coverage can be achieved.

3.1 Test Processor Architecture

The functional block diagram of the IC test processor implementing GLFSR based mixed-mode technique is shown in Figure 4. It consists of micro-UART, control unit, GLFSR, Signature Analyzer (SA), Buffer Register (BR), Information Register (IR), and Random Access Memories (RAMs). Prior to start testing of a CUT, necessary test information is loaded from PC through micro-UART. The information register (IR), test length storage RAM (TL_R), seed storage RAM for random test pattern generation (SD_R), seed storage RAM for deterministic test pattern generation (SDD_R) and signature storage RAM (SG_R) are used to store the test data. Once data loading is completed, testing process is 'ON'. During testing process, test vectors are generated from the GLFSR and are loaded into the BR and are applied to the CUT. Output response of the CUT is captured into the BR and sent to the SA. At end of the test set, the generated signature is compared with that of a fault-free circuit of the same type (reference CUT). If the two signatures are the same, then the CUT is determined as fault-free, otherwise as faulty.

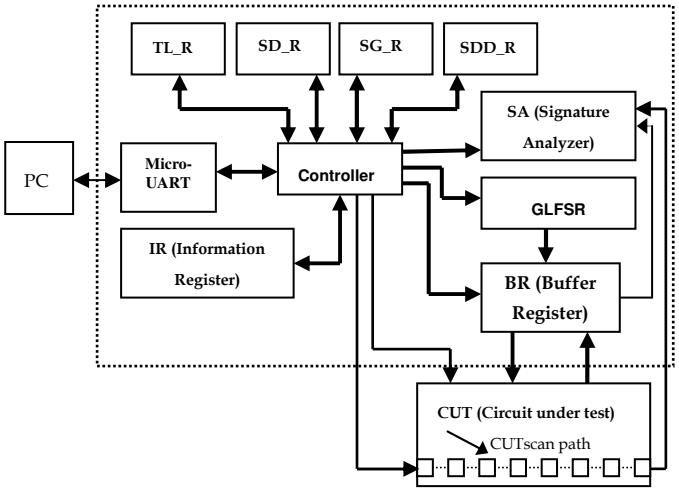


Figure 4: Functional block diagram of the proposed test processor.

3.2 Testing Procedure

The operation of the IC tester has three phases: (a) load data in the IR and the RAMs (b) circuit test and (c) retrieval of test result. Prior to start testing of a CUT the IR, TL_R, SD_R and SDD_R are loaded with appropriate information from PC through micro-UART. In the mixed-mode testing, pseudo-random testing approach is followed by deterministic testing approach. To start pseudo-random testing of the CUT, the controller reset the GLFSR, the BR, and the SA to zero and reads the test length, the seed and the signature from the TL_R, SD_R, and SG_R respectively. The GLFSR is initialized with the seed and generates PRV. The PRV is loaded into the BR and scan path (SP) and then applied to the CUT. The output response vectors of the CUT are captured into the BR and that of secondary output of the CUT into the SP. When the test vectors of the second test cube are loaded into BR and SP, output responses of the CUT due to the first test cube are shifted into the SA. The controller of the tester counts the number of test cubes of PRV applied to the CUT. The testing process continues until the test count equal to the predefined test length for the pseudo-random test. Once the pseudo-random test is completed, the deterministic test starts. The controller reads the seed from the SDD_R and generates deterministic test cube by decoding the seed using the GLFSR. The test cube is applied to the CUT and the output response vectors are captured into the BR and sent to the SA in the same fashion as that of the pseudo-random testing. The controller counts the number of deterministic test cubes applied to the CUT. When the number of the test cubes equals to the predefined number of deterministic test length then the generated signature is compared with that of the reference signature and the status of the CUT is determined as fault-free if the two signatures are the same otherwise as faulty. The procedure of testing is illustrated below:

1. *Load IR with necessary information about the CUT and Number of test sets.*
2. *Read data for test length signature and seed*
3. *Generate test vector and apply to CUT*
4. *Capture output response of CUT and send to SA*
5. *If the number of test vector is no equal to number of predefined test length then go to step 3.*
6. *Compare signature and determine whether the IC is fault free on not.*
7. ***If** the number of test set is not equal to presetted number of test set the go to step 3 else end of test*

4 Fault Simulation Results

Fault simulation experiments have been conducted using FSIM digital fault simulator on ISCAS85 benchmark circuits. Summary of the fault simulation results using GLFSR based mixed-mode approach is shown in Table 1.

TABLE 1
SUMMARY OF THE FAULT SIMULATION RESULT OF ISCAS85 BENCH-MARK CIRCUIT USING GLFSR BASED MIXED MODE APPROACH

Benchmark Circuit	No of Faults	Patterns required	Fault Coverage
c432	524	214	100%
c499	758	225	100%
c880	942	248	100%
c1355	1574	314	100%
c1908	1879	969	100%
c2670	2747	724	100%
c3540	3428	271	100%
c5315	5350	388	100%
c6288	7744	234	100%

The table shows that the total number of test vector including deterministic required achieving complete fault coverage for ISCAS benchmark circuit. It shows that 100% fault coverage can be achieved using mixed-mode approach. The result presented in Table 1 can be compared with that of other researchers [7, 8, 9, 11 and 14]. Comparison of the fault simulation result is presented in Table 2.

TABLE 2
COMPARISONS OF FAULT SIMULATION RESULTS OF THE ISCAS85 BENCHMARK CIRCUITS WITH THAT OF OTHER RESEARCHERS

Benchmark Circuit	*TV1	*TV2	*TV3	*TV4	*TV5	*TV6	*TV7
C432	214	232	352	320	512	1024	320
C499	225	518	-	-	-	-	-
C880	248	179	4544	416	260	1280	160
C1355	314	526	1248	1664	2244	2098	2784
C1908	969	996	4608	2496	2308	5376	3916
C2607	724	360		6240	10766	5888	6400
C3540	271	748	1065	9504	12220	3840	4352
C5315	388	662	1632	1950	1316	2048	1024
C6288	234	69	-	-	-	-	-

*TV1: Number of test vectors required in the present work

*TV2: Number of test vectors using DRM mixed-mode technique obtained by Liakot (2004)

*TV3: Number of test vectors using MP-LFSR based mixed-mode technique obtained by Liakot (1998)

*TV4: Number of test vectors using weighted random technique obtained by Iftekhar (1995)

*TV5: Number of test vectors using weighted random technique obtained by Wunderlich (1990)

*TV6: Number of test vectors using weighted random technique obtained by Waicukauski et al. (1989)

*TV7: Number of test vectors using weighted random technique obtained by Lisanke et al. (1990).

The sign '-' in Table 2 indicates the unavailability of the actual data. It shows that the proposed GLFSR based mixed-mode approach is capable conducting IC testing with 100% fault coverage using much lower number of test vectors that that of other researchers.

5 CONCLUSION

A novel pattern generator GLFSR based test processor has been presented in this paper. In this testing mixed-mode approach has been implemented for IC testing. The detail design of the test processor and testing procedure are discussed. The proposed approach can test IC effectively with reasonable fault coverage and have the potential to detect faults effectively. The test patterns generated by the proposed method are applied to the ISCAS bench mark circuits. The fault simulation results show that the proposed approach requires much fewer patterns than other approaches. This can be significance for the faults detection of very large circuits with a large number of inputs.

REFERENCES

[1]. D. K. Pradhan, S. K. Gupta, "A new framework for designing & analyzing BIST techniques and zero aliasing compression", *IEEE Transactions on Computers*, 40, pp.743-763, 1991.

[2]. R. Rajsuman, *System-on-a-chip: Design and Test*, Artech House, Boston, 2000.

[3]. L. Ali, R.Sidek, I. Aris, M. A. Mohd. Ali, and B. S.Suparjo, *Challenges and Directions for IC testing, Integration,*The VLSI Journal, pp. 17-28, Vol 37(1), Elsevier Science, Netherland,2004.

[4]. Nadeau_Dostie, "Design for At-speed Test, Diagnosis and Measurement", K. A. Publisher, Boston USA, 2000.

[5]. R. W. Bassett, B. J. Butkus, Dingle et al.,"Low cost testing of high density logic components", *Proceedings of International Test Conference*, pp. 550-557, 1989.

[6]. N. Jarwala, and C. W. Yau, "Achieving board-level BIST using the boundary-scan master",*IEEE Proceedings of International Test Conference* pp. 649-658, 1991.

[7]. A. P.Strole, and H. J. Wunderlich, *TESTCHIP: A chip for weighted random pattern generation, evaluation and test control,* IEEE Journal of Solid-State Circuits, pp. 1056-1063, 1991.

[8]. I. Ahmed, VLSI circuits testing using probabilistic approach, Ph.D. Diss., UniversitiKebangsaan Malaysia,1995

[9]. J. A. Waicukauski, E. Lindbloom, E. B. Eicheblberger and O. P. Forlenza, *A method for generating weighted random test patterns*, IBM Journal of research and development Vol. 33(2):149-161, 1989.

[10]. J. A.Waicukauski, and E. Lindbloom, "Fault detection effectiveness of weighted random patterns,"*Proceedings of International Test Conference, pp. 245-255*, 1988.

[11]. L. Ali, Development of a functional digital integrated circuit testing system using mixed-mode technique. Ph.D. Thesis, Universiti Putra Malaysia, 2004.

[12]. L. Ali, R. Sidek, I. Aris, R.Wagiran, M. A. Ali, and B. S. Suparjo, "Development of FPGA-based functional IC Testing System", *ROVISP'2005*, Penang, Malaysia,2005.

[13]. C. V. Krishna, A. Jas, and N. A. Touba, "Test vector encoding using partial LFSR reseeding,"*In Proceedings of International Test Conference*, pp. 885-893, 2001.

[14]. L. Ali, Design of a processor chip using multiple polynomial, multiple seed linear feedback shift register. M.Sc. Thesis, UniversitiKebangsaan Malaysia, 1998

[15]. S. Hellebrand, S. Tarnick, J. Rajski, and B. Courtois, "Generation of vector patterns trough reseeding of multiple–polynomial linear feedback shift registers," *IEEE Proceedings Of International Test Conference*, pp. 120-129, 1992.

[16]. S. Hellebrand, S. Tarnick, S. Venkataraman, and B. Courtois, "Built-in test for circuits with scan based on reseeding of multiple–polynomial linear feedback shift registers,"*IEEE Trans. on Comp. Vol.* 44(2), pp. 223-233, 1995.

[17]. D. K. Pradhan, M. Chaterjee, "GLFSR- a new test pattern generator for built-in-self-test'"*IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume* 18(2), pp. 238-247, 1999.

Mohammod Akbar Kabir received his M.Sc. and B.Sc.(Hons.) in Computer Science from the University of Dhaka in 2000 and 1998, respectively. Currently he is working as an Assistant Professor at the Dept. of Economics, University of Dhaka. He also served as an Assistant Programmer at the Dept. of ITOCD, Bangladesh Bank and as a Lecturer, Dept. of Computer Science, Dhaka City College. His research interests are in the area of VLSI Design and E-Commerce.

Md. Nasim Adnan received M.Sc. in CSE from Bangladesh University of Engineering and Technology (BUET) and B.Sc. in CSE from Khulna University. Currently he is working as an Assistant Professor in the Dept. of Computer Science and Engineering, University of Liberal Arts Bangladesh (ULAB). He also served as a Deputy Director in the Dept. of ITOCD, Bangladesh Bank. His research interest includes Data Mining, Database Systems, Software Engineering, Software and Systems Testing, and E-Commerce.

Lutful Karim has been working as a faculty member of Computer Science in Islamic University of Technology (IUT) since 2000. Now, he is a Ph.D. student at the University of Guelph in Canada. He has authored several refereed conference and journal publications, and been a member of organization committee and technical program committee in several international conferences. His research interest includes Wireless Communications, Wireless Sensor Network, Fault Tolerance and E-Commerce.