Impact of Temperature on Threshold Voltage of Gate-All-Around Junctionless Nanowire Field-Effect Transistor

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Abstract—Commonly used transistors are based on the use of semiconductor junctions formed by introducing doping atoms into the semiconductor material. As the distance between junctions in modern devices drops below 10 nm, extraordinarily high doping concentration gradients become necessary. For this reason, a new device was proposed which has full CMOS functionality and is made by using junctionless nanowires. They have near-ideal sub-threshold slope, extremely low leakage currents and less degradation of mobility with gate voltage and temperature than classical transistors. Among several types of field effect transistors, gate-all-around junctionless nanowire FET (GAA-JL-NW-FET) is the recently invented one. In this article, temperature dependency of threshold voltage of GAA-JL-NW-FET has been analyzed for different channel materials such as Si, GaAs, InAs and InP. From the simulation result, it is observed that the threshold voltage is minimum for InAs and it decreases when the temperature is increased for all the above mentioned channel materials.

Keywords—Gate-All-Around, Junctionless, Nanowire, Temperature dependency, Threshold voltage.

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1 Introduction

NANOELECTRONIC devices have been used in very extreme environments like low temperature ranges as well as high temperature ranges. So their behavior in response to temperature has attractted the attention of researchers. Different studies and investigations are going on to understand the performance of all types of transitors in different temperatures. Threshold voltage, one of the major parameters that can be influenced very easily by temperature change, has been taken under consideration in this article [1].

The existing transistors are based on the formation of junctions. Junctions are capable of both blocking current and allowing it to flow, depending on an applied bias. The most common junction is the p-n junction. Other types of junctions include the metal-semiconductor 'Schottky' junction and the heterojunction, which is a p–n junction comprising two different semiconductor materials. The bipolar junction transistor (BJT) contains two p-n junctions, and so do the metal-oxide–semiconductor field-effect transistor (MOSFET) and most of the modern transistors. The junction field-effect transistor (JFET) has only one p–n junction and the metal–semiconductor field-effect transistor (MESFET) contains a Schottky junction.

Conventional MOSFETs are usually fabricated on a semiconductor bulk substrate. With the continuous scaling of the device dimension, these bulk MOSFETs are facing serious challenges, such as the increasing gate leakage current and more serious short channel effects [2]. Gate-all-around (GAA) nanowire (NW) transistors are regarded as a promising device structure to extend the scaling limit due to their superior gate controllability. On the other hand, the formation of the abrupt source and drain junctions in the conventional NW devices imposes severe challenges on doping techniques and thermal budget [3]. As an alternative, junctionless (JL) devices with a uniform doping concentration and type throughout the channel and source/drain extensions are fabricated to overcome these challenges.

In recent times transistors have become of nanometer sizes, due to the aggressive scaling. At this size it is very hard to control the sharp source/drain-channel junctions from the device fabrication point of view. Also many other unwanted effects such as gate leakage, short channel effects, hot carrier effects etc. have been seen to be increasing. For reducing the short channel effects the GAA-FETs are the best since they provide the best control over the channel from all around [4]. But if channel with corners, i.e. rectangular shape, is used for this purpose then it leads another effect known as corner effect [5]. To avoid this, cylindrical structure looks to be promising and has been widely used for getting rid of corner effect and also to improve other short channel effect performance parameters.

The first JL transistor was introduced back in 1920s [6], [7], but it has attracted researches recently. JL transistors are inherently depletion mode devices and needs a gate voltage to be applied to make them OFF [8]. One advan-

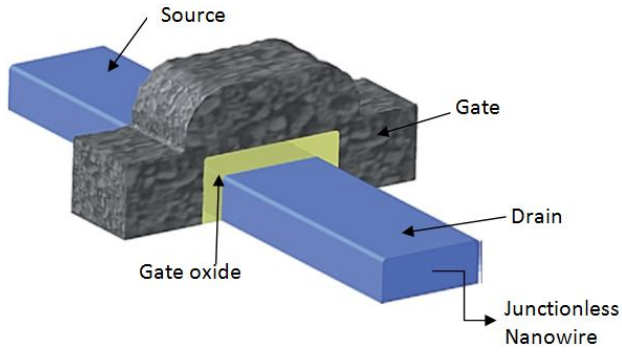

Figure 1: Schemetic view of a JL-NW-FET. Here souce, channel and drain are consists of a single JL NW. The underlying insulator (buried oxide) is not shown [10].

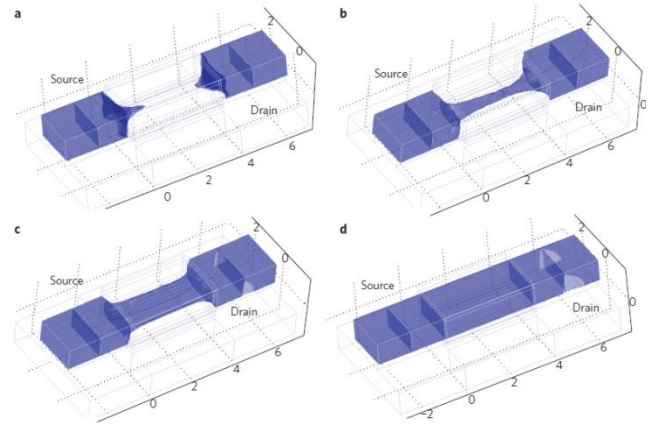

Figure 2: Electron concentration contour plots in an n-type junctionless gated resistor. a–d, Plots result from simulations carried out for a drain voltage of 50 mV and for different gate voltage (V_G) values: below threshold ($V_G<V_{TH}$) the channel region is depleted of electrons (a); at threshold ($V_G=V_{TH}$) a string-shaped channel of neutral n-type Si connects source and drain (b); above threshold ($V_G>V_{TH}$) the channel neutral n-type Si expands in width and thickness (c); when a flat energy bands situation is reached ($V_G=V_{FB}>>V_{TH}$) the channel region has become a simple resistor (d). The plots were generated by solving the Poisson equation and the drift-diffusion and continuity equations self-consistently. The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1×10^{19} cm^{-3} [10].

tage of these are that it operates due to the conduction of carriers in bulk as opposed to the conventional MOSFETs (inversion mode devices), in which the carriers conducts through a thin layer of inversion charge layer created at the oxide-semiconductor interface. Hence, the current driving capability is improved a lot. However, it is also degraded slightly due to the high doping concentrations used in the channel.

2 GAA-JL-NW-FET

2.1 NW-FET

Semiconductor NWs have attracted significant interest because of their potential for a variety of different applications, including logic and memory circuitry, photonic devices, and chemical and biomolecular sensors [9].

2.2 JL-NW-FET

Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms, conventional junctions represent an increasingly difficult fabrication challenge for the semiconductor industry. A new type of transistor has been proposed and demonstrated in which there are no junctions and no doping concentration gradients [10]. These devices have full CMOS functionality and are made using NWs. They have near-ideal subthreshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors.

Figure 1 presents a schematic view of a JL-NW-FET. Having no junctions presents a great advantage. Modern transistors have reached such small dimensions that ultra sharp doping concentration gradients are required in junctions. Typically the doping must switch from n-type with a concentration of 1×10^{19} cm^{-3} to p-type with a concentration of 1×10^{18} cm^{-3} within a couple of nanometers. This imposes severe limitations on the processing thermal budget and necessitates the development of costly millisecond annealing techniques. In a JL gated resistor, on the other hand, the doping concentration in the channel is identical to that in the source and drain. Because the gradient of the doping concentration between source and channel or drain and channel is zero, no diffusion can take place, which eliminates the need for costly ultrafast annealing techniques and allows one to fabricate devices with shorter channels. The key of fabricating a JL gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations.

In a MOSFET, carriers are confined in an inversion channel in which scattering events rapidly increase in frequency with gate voltage, thereby decreasing transconductance and current drive [11]. In the heavily doped gated resistor, the drain current essentially flows through the entire section of the nano-ribbon, instead of being confined in a surface channel. Figure 2 shows the electron concentration in an n-type JL gated resistor for different values of gate voltage ranging from device pinch-off (Figure 2a) to flat-band conditions (Figure 2d). The conduction path is clearly located near the centre of the NW, not at the semiconductor-oxide interface. This allows the electrons to move through the core of the channel with bulk mobility, which is influenced much less by scattering than the surface mobility experienced by regular FETs. It is possible to create surface accumulation channels by increasing the gate voltage beyond the flat-band voltage, if a further increase of drain current is desired [10]. Because it operates under bulk conduction rather than channel conduction, the gated resistor sees its transconductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance, can be expected from the gated resistor.

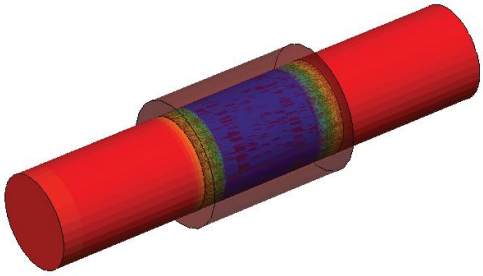

Figure 3: Structure of cylindrical GAA-JL-NW-FET [12].

2.3 GAA-JL-NW-FET

The JL-NW-FET, as illustrated in figure 3, has become widely recognized as one of the most promising candidates for future nanoscale CMOS technology due to its excellent subthreshold slope (SS), low drain-induced barrier lowering (DIBL) and low leakage current [12]. But it has a limitation which is related to the carrier transportation or mobility. In general, carrier transport can be divided into three regimes: diffusive transport, ballistic transport, and quantum transport [13]. When the gate length is much greater than the carrier mean free path, the carriers transit within the diffusive transport regime where scattering dominates. Carriers can reach their equilibrium states through sufficient scattering events and thus Drift-Diffusion (DD) model can capture well this equilibrium carrier transport property. When the gate length is shorter than de Broglie wavelength [14], the carriers transit within the quantum transport regime, where the full quantum transport approach such as Non Equilibrium Green Function (NEGF) is suitable to simulate strong quantum confinement and significant source to drain tunneling. In the range between these two regimes, the carriers transit from quasi-ballistic to ballistic transport regime. The semi-classical approach Monte Carlo simulator incorporated with full band structure is able to capture the non-equilibrium transport effects [15].

Figure 4 depicts the GAA-JL-NW-FET with its circular cross-sectional and top views [16].

3 Temperature Effect on Threshold Voltage

For an enhancement mode, n-channel MOSFET body effect upon threshold voltage is computed according to the Shichman-Hodges model. This model was accurate for the devices having channel lengths in the range of microns [17].

$$V_{TH} = V_{T,0} + \gamma\left(\sqrt{|V_{SB} + 2\varphi_F|} - \sqrt{|2\varphi_F|}\right)$$

where V_{TH} is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, $2\varphi_F$ is the surface potential, and $V_{T,0}$ is threshold voltage for zero substrate bias, $\gamma = (t_{ox}/\varepsilon_{ox})\sqrt{2q\varepsilon_S N_A}$ is the body effect parameter, t_{ox} is oxide thickness, ε_{ox} is the relative permittivity of oxide, ε_S is the relative permittivity of semiconductor, N_A is a doping concentration, q is the charge of an electron.

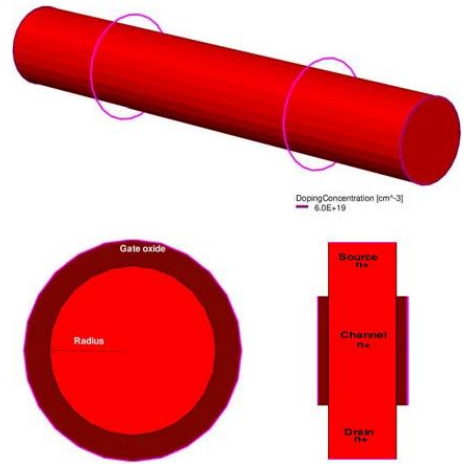

Figure 4: 3D structure of GAA-JL-NW with their cross-sectional views (both side and top views) [16].

As with the case of oxide thickness affecting threshold voltage, temperature has an effect on the threshold voltage of a CMOS device. Expanding on part of the equation in the body effect section,

$$\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

where φ_F is half the contact potential, k is Boltzmann's constant, T is Temperature and n_i is the intrinsic doping parameter for the substrate. And it is known that [18],

$$n_i = 5.2\times10^{15}\times T^{3/2}\times\exp\left(-\frac{E_g}{2kT}\right)$$

Here E_g is the bandgap energy of the channel material.

It can be seen that the surface potential has a direct relationship with the temperature. Looking above, that while the threshold voltage does not have a direct relationship but is not independent of the effects.

The variation of the threshold voltage of a gated resistor with temperature is similar to that of a bulk MOSFET, with values of approximately –1.5 mV°C^{-1} measured in these devices. Interestingly, the decrease of mobility with temperature is much smaller in the gated resistors than in tri-gate FETs. In a lightly doped FET, the mobility is little affected by impurity scattering and tends to be phonon limited, so it shows a strong temperature dependence. In the highly doped gated resistor, on the other hand, mobility is limited by impurity scattering rather by phonon scattering, and its variation with temperature is much smaller. For instance, the electron mobility measured at room temperature in tri-gate FETs and gated resistors is 300 and 100 cm^{2}V^{-1}s^{-1}, respectively. When heated to 200 °C, the tri-gate FETs show a 36% loss of mobility, whereas the gated resistor has a reduction in mobility of only 6% [10].

For GAA-JL-NW-FET, the equation stands for the threshold voltage depends upon the work function, radius of device, thickness of oxide and the permittivity of oxide and material that is used [19].

$$V_{TH} = \Delta\varphi + \frac{kT}{q}\ln\left(\frac{8\mathrm{kT}\varepsilon_S}{q^2 n_i}\right) - \frac{2kT}{q}\ln\left[R\left(\frac{1+t_{ox}}{R}\right)^{\left(\frac{2\varepsilon_S}{\varepsilon_{ox}}\right)}\right]$$

Where, $\Delta\varphi$ is the work function difference and R is the radius of the device.

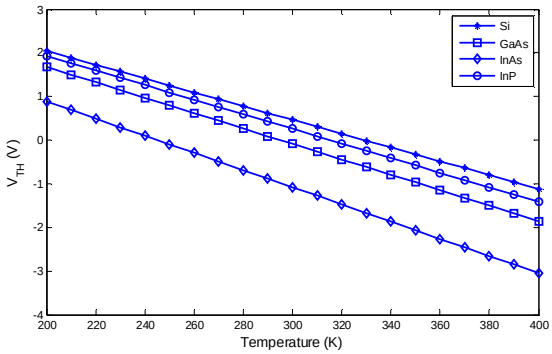

Figure 5: V_{TH} vs. temperature of GAA-JL-NW-FET. Four different matrials, Si, GaAs, InAs and InP, have been considered for the analysis.

4 Simulation and Result

In this article, the change of threshold voltage of GAA-JL-NW-FET having channel of different materials as a function of temerature has been simulated using MATLAB and then analyzed. Before the simulation, careful approximations should be made regarding the device dimentions of the GAA-JL-NW-FET. The parameters have already been approximated in different research works. From those, suitable estimated have been selected for this article [16].

The radius of the NW and the oxide-thickness are considered to be 2.5 nm and 0.77 nm, respectivey. The relative permittivity of the gate-oxide, considering SiO_2, has been taken as 3.9. And the workfunction difference has been approximated as 4.63 V.

For the analysis, four different channel materials have been considered, Si, GaAs, InAs and InP. The bandgap energies of these materials are 1.12 eV, 1.42 eV, 0.36 eV and 1.27 eV, respectively, and their relative permittivities are 11.7, 13.1, 14.6 and 12.4, respectively [20].

Considering the above mentioned values along with the general constants the simulation has been run over the temperature range of 200 K to 400 K. Threshold voltage versus temperature curve has been shown in figure 5.

From this figure it can be seen that for all the above metioned materials the threshold voltage reduces if the temperature is increased. And over the 200 K range, the change in threshold voltage is significant, around 3 to 4 V.

It means, if the temperature of the environment is as low as 200 K, they have a threshold voltage of 1 to 2 V. Whereas, at around 400 K temperature their threshold voltage become around –1 to –3 V. This result indicates that, if the temperature rises, the devices need less gate-voltage to be turned ON. It can be an important finding regarding in which applications they can be utilized.

Furthermore, at room temperature, i.e., 300 K, the threshold voltage of the experimented Si-channel GAA-JL-NW-FET is 0.4639 V. Device having GaAs-channel has the threshold voltage of –0.0865 V at room temperature. For InAs-channel transistor at 300 K, the threshold voltage is –1.0804 V. And if the channel is of InP, the threshold voltage is 0.2580 V at room temperature.

These results are clear indications of the material dependancy of threshold voltage of GAA-JL-NW-FET. The lowest threshold voltage can be achieved from InAs and the highest from Si. It proves the fact that, using a channel material with higher bandgap energy ensures a higher threshold voltage and vice versa. Keeping these in mind, the channel materials should be chosen so that they can accomplish the necessity.

5 Conclusion

GAA-JL-NW-FET is one of the most promising transistors for the near future for its simplicity and other electronic properties like near-ideal sub-threshold slope, extremely low leakage currents and less degradation of mobility with gate voltage and temperature than classical transistors. However, the high doping concentration in the channel reduces carrier mobility, which hurts drive current and transconductance of JL MOSFETs.

The temperature effect on the threshold voltage of this device has been deeply investigated over a range of 200 K to 400 K. And from this analysis, a conclusion may be drawn that the threshold voltage of GAA-JL-NW-FET is temperature dependant and it decreases with the increament of temperature.

The study has been made for Si, GaAs, InAs and InP NW based devices. From this study, it is clear that the minimum and maximum threshold voltages are achieved using InAs and Si, respectively.

It has already been mentioned earlier that GAA-JL-NW-FET has a great potential to replace the existing transistors. It is very important for the researchers to study its different characteristics for proper utilization. In the near future, the properties of this device along with the use of different channel materials may be studied.

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